INSTITUT D'ELECTRONIQUE ET DE TELECOMMUNICATIONS DE RENNES

Field effect transistor sensors for liquid media

Water micropollutants: from detection to removal

November 26-28, 2018
Orléans

IETR

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OUTLINE

- Some liquid sensors
- Dual Gate FET
  - Examples
  - Process of Dual Gate TFT
  - Theory
- Characterization
- Tests for PH measurement
- Prospects

Water sensors

- Some measure parameter
  - Temperature
  - pH
  - conductivity
  - dissolved oxygen
  - turbidity........
- Sensor principle
  - Thermistor
  - Redox sensor
  - Metallic electrodes
  - Electrochemical or optical
  - Optical measurement of diffuse light

PH sensors

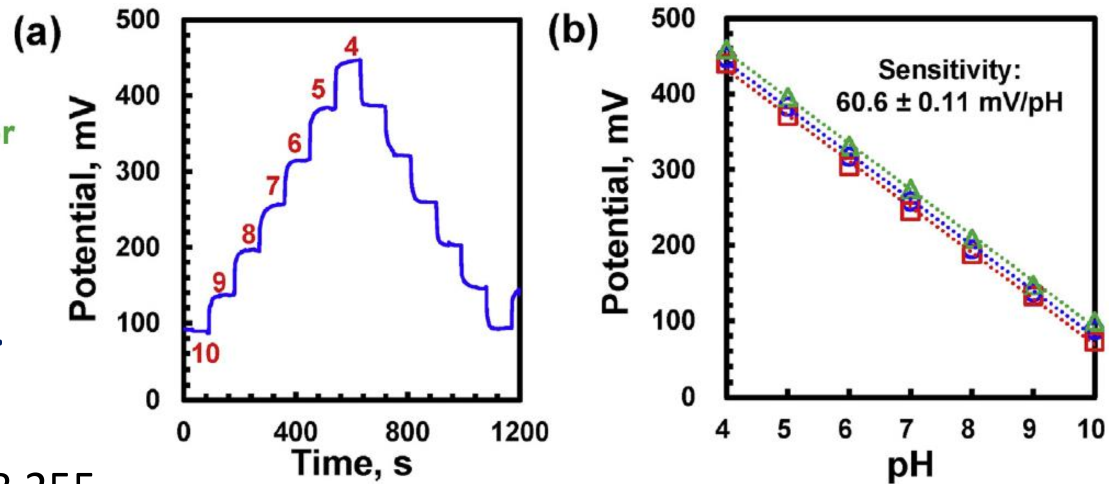
- Equation :
  - Ox1 + Réd2 <-> Réd1 + Ox2

$$E = E^0 + \frac{RT}{nF} ln(\frac{a_{ox}}{a_{red}})$$

(Nernst equation)

$$E = E'^0 + 0,059.log([H^+])$$

$$E = E'^0 + 0.059.pH$$



  - $PdO + 2H^+ + 2e^- \leftrightarrow Pd + H_2O$.

Y. Qin et al. / Sensors and Actuators B 255 (2018) 781–790

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Sensors objective

- Developing high sensitive sensors from:
  - Electronic device
  - Compatible technologies
  - Easy to functionalize

→

- Field effect transistors:
  - Detection of charges linked to the surface
  - Easy measurement
  - Numerous possibilities for the technology
  - Low cost and high number of devices

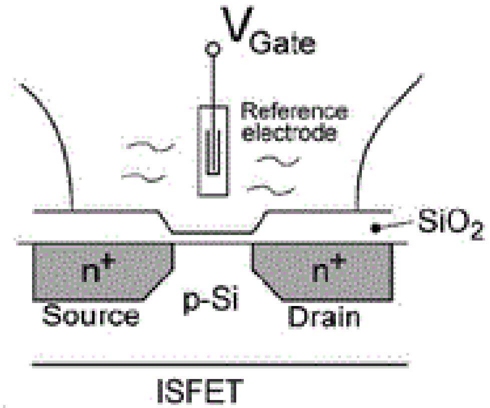
- Specialized in silicon based technologies:
  - Thin film devices
  - Low temperature process
  - Good electrical properties

→

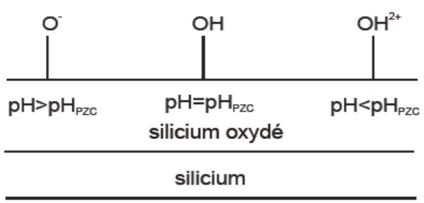
- TFT as chemical sensors:
  - Different technologies
  - Compatibility with chemical and biological functionalization
  - Possibility to integrate microfluidic
  - Usable in liquid media
  - Highly sensitive devices

Main principle silicon based sensors

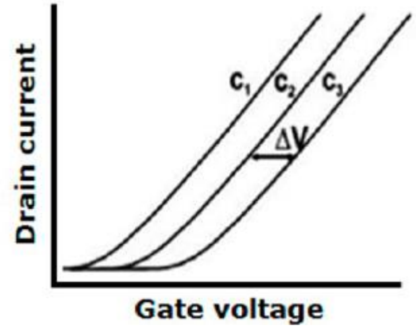
- **ISFET : Ions Sensitive Field Effect Transistors**



→ pH sensor



pH_{pzc} : isoelectric pH



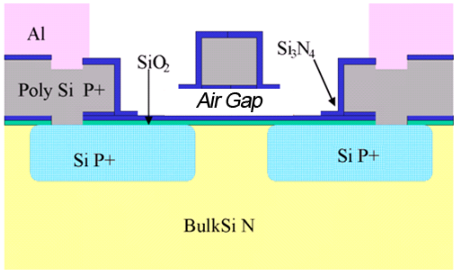
pH variation : shift of the transfer characteristic and of the threshold voltage

Sensitivity: $S = \frac{d\Psi}{dpHs} = -2{,}3\,\frac{kT}{q}\,\boldsymbol{\alpha}$ S= 59 mV/pH (Nernst equation)

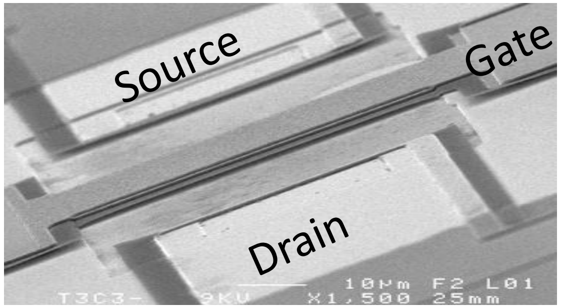
Well-know device with main advantages → Limitation of the sensitivity

Main principle silicon based sensors

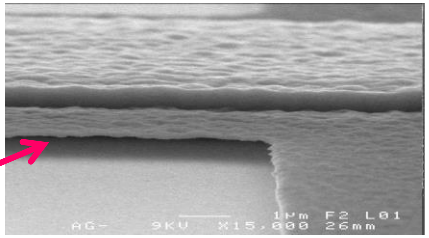
- SGFET : Suspended Gate Field effect Transistor



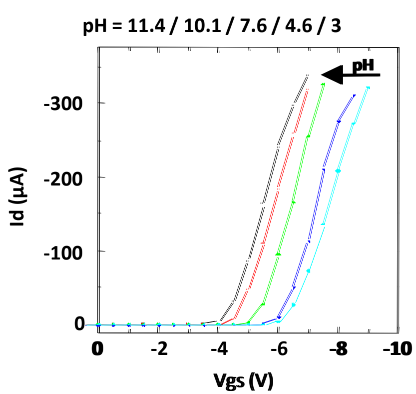
MOS or TFT structure
With suspended gate

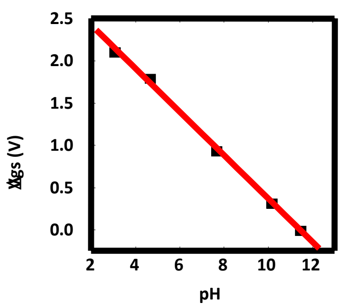


Sub-Micron Gap
(300-800 nm)



Compatible with measurements in liquid media
→ pH sensor (Si_3N_4 layer)





Sensitivity : ΔV_{gs}/pH = 255 mV / pH

Biosensors

- Chemical and biological functionalization
- Antigens/Antibodies

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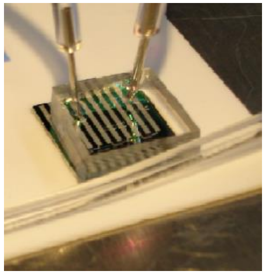
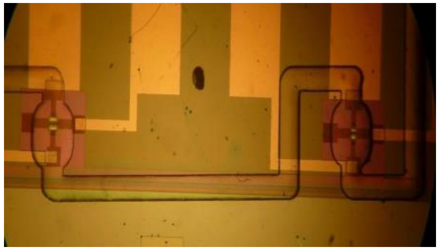
Microfluidics integration

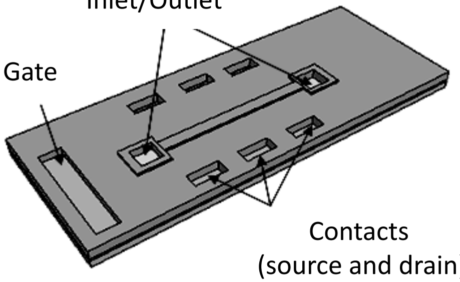
With PDMS microchannels

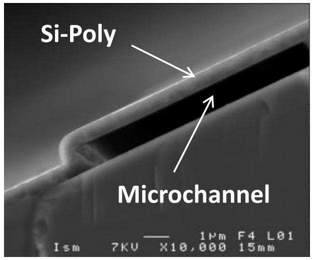
Control of the volume
Continuous flow
Same sensitivity

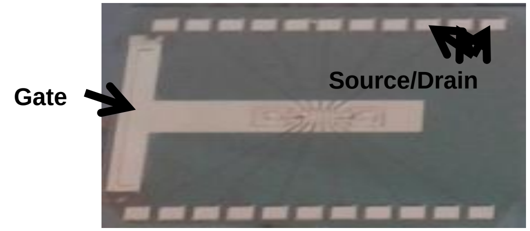


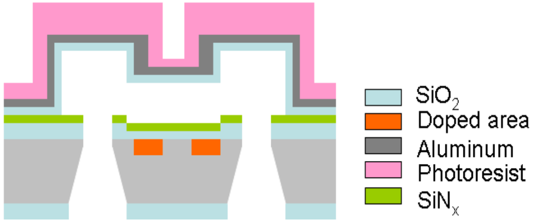


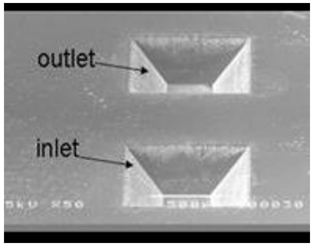
With integrated microchannels (front or rear face)

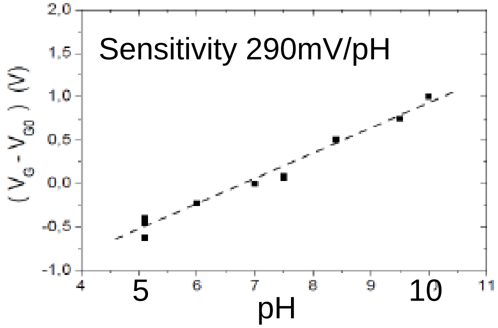












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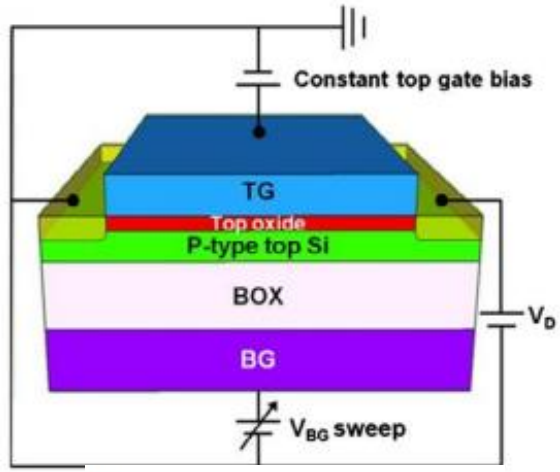
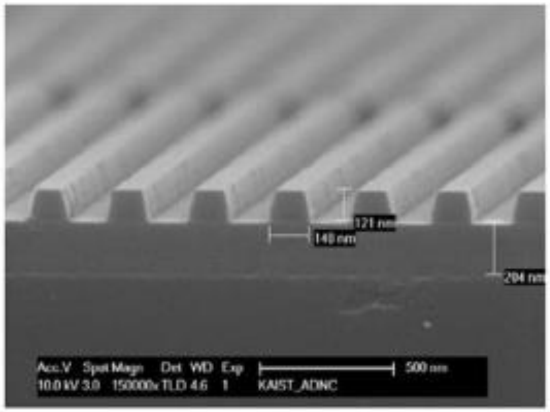
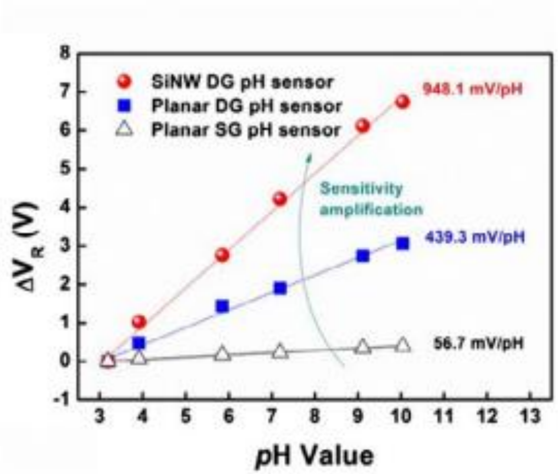
DGFET : Example 1

Improved sensing characteristics of dual-gate transistor sensor using silicon nanowire arrays defined by nanoimprint lithography

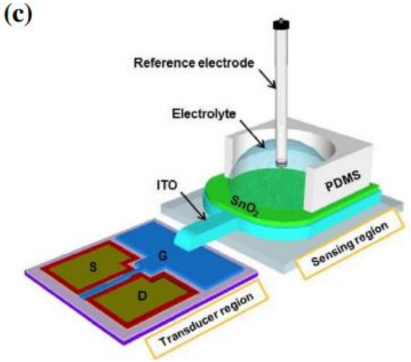
Lim *et al*, Science and Technology of Advanced Materials, 2017 VOL. 18, NO. 1, 17–25







(c)



- nanoimprinted SiNW for the active layer
- Silicon dioxide
- Extended gate

→ High sensitivity

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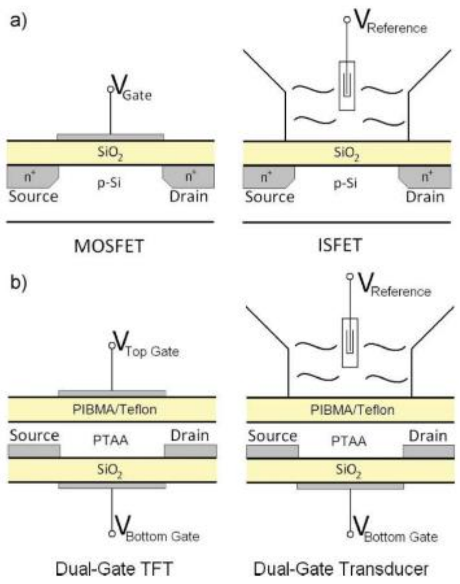
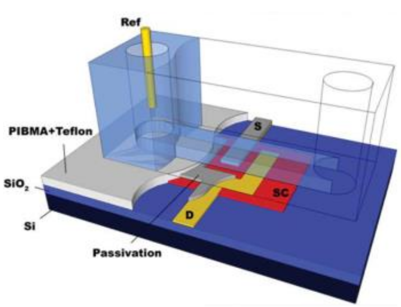
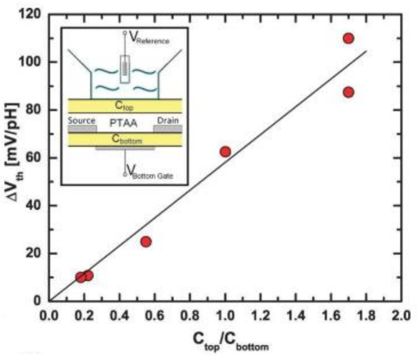
DGFET : Example 2

Dual-Gate Organic Field-Effect Transistors as Potentiometric Sensors in Aqueous Solution
By Mark-Jan Spijkman, *et al*, Adv. Funct. Mater. 2010,20,898–905





- PTAA stands for the organic semiconductor polytriarylamine.
- The top dielectric consists of a stack of poly-isobutylmethacrylate (PIBMA) and the Teflon derivative AF-1600.



Sensitivity to pH
versus coupling capacitance

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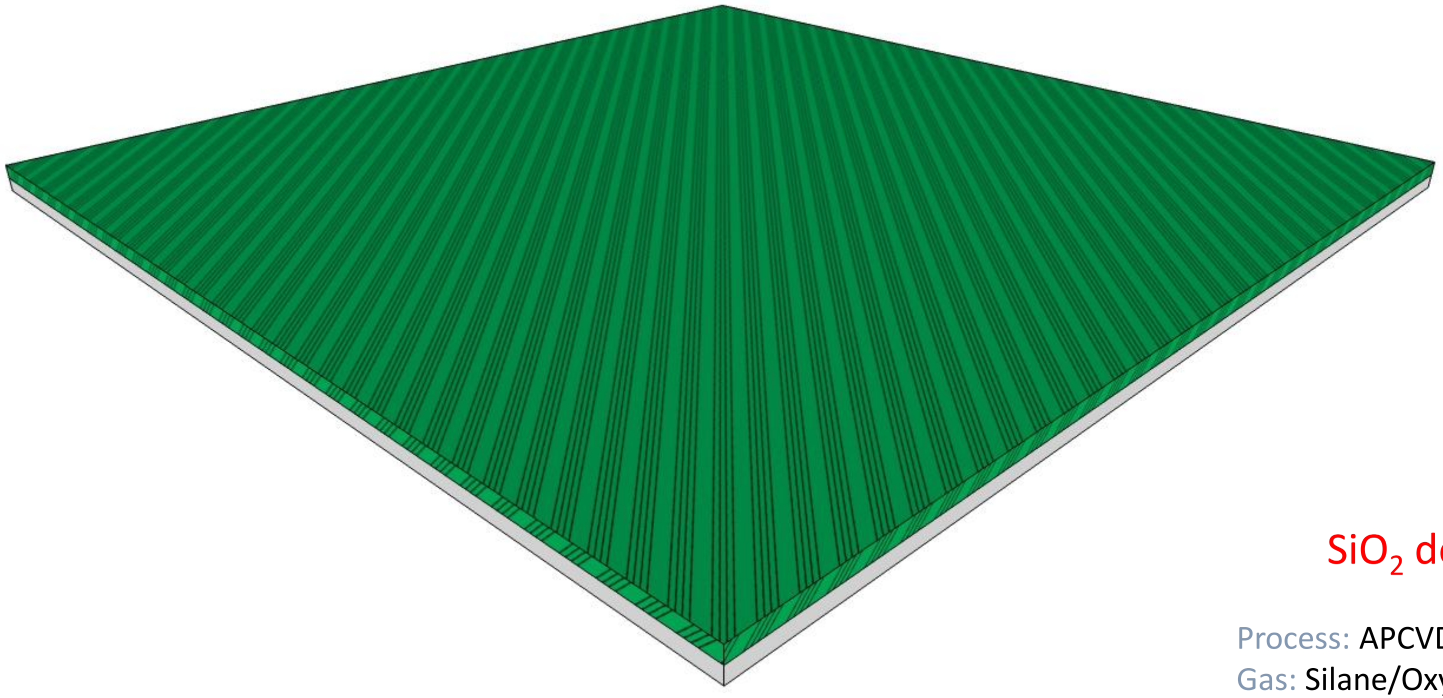
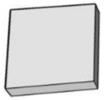
Dual Gate TFT with polysilicon



SiO$_2$ deposition

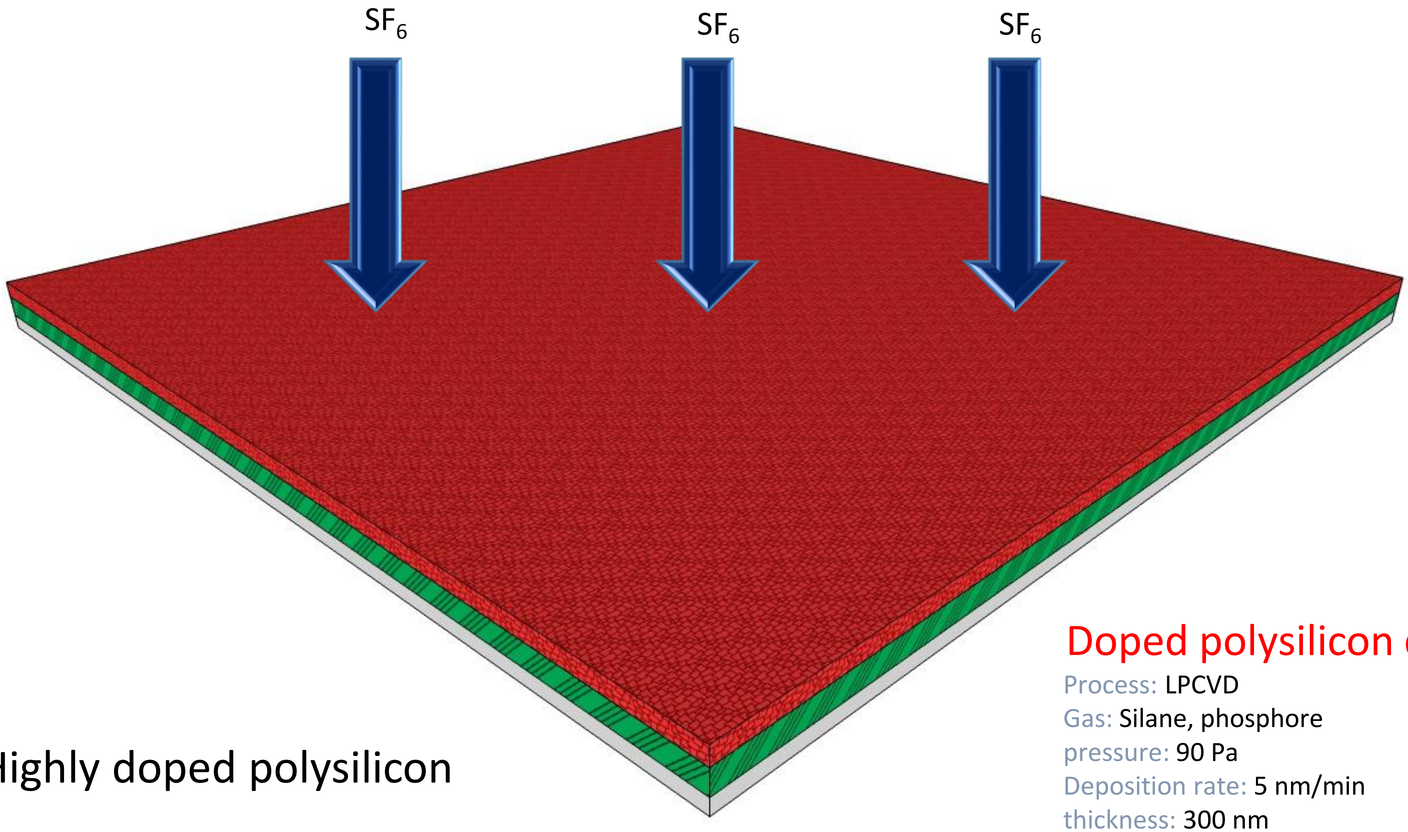
Process: APCVD
Gas: Silane/Oxygene
Temperature: 420°C
Deposition rate: 29 nm/min
Thickness: 800 nm

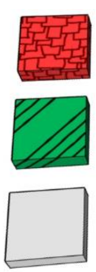
Wafer insulation (silicon oxide)



Silicon Wafer

Dual Gate TFT with polysilicon





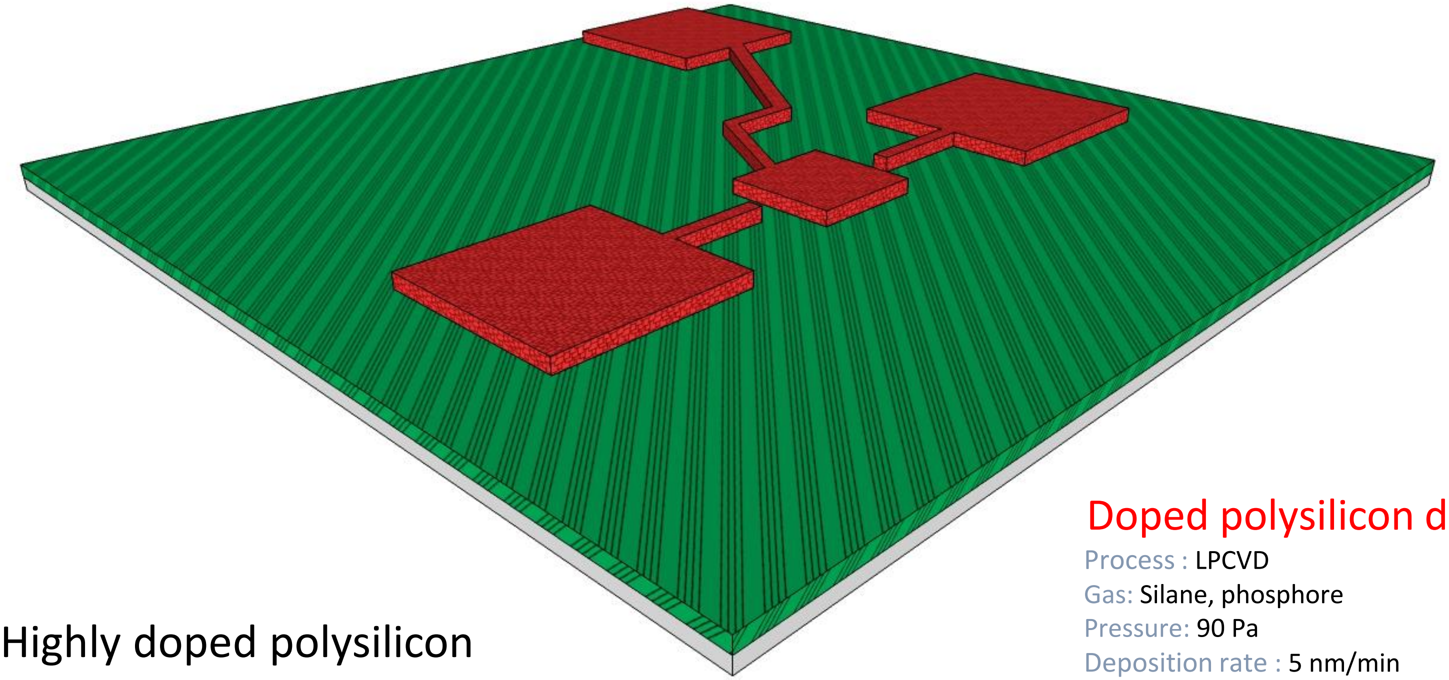
Doped polysilicon deposition

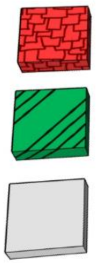
Process: LPCVD
Gas: Silane, phosphore
pressure: 90 Pa
Deposition rate: 5 nm/min
thickness: 300 nm

Dry etching

Process : Plasma
power: 30w
Flow rate: 30sccm
pressure: 4 Pa
Etching rate: ~150nm/min

Dual Gate TFT with polysilicon





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Dry etching

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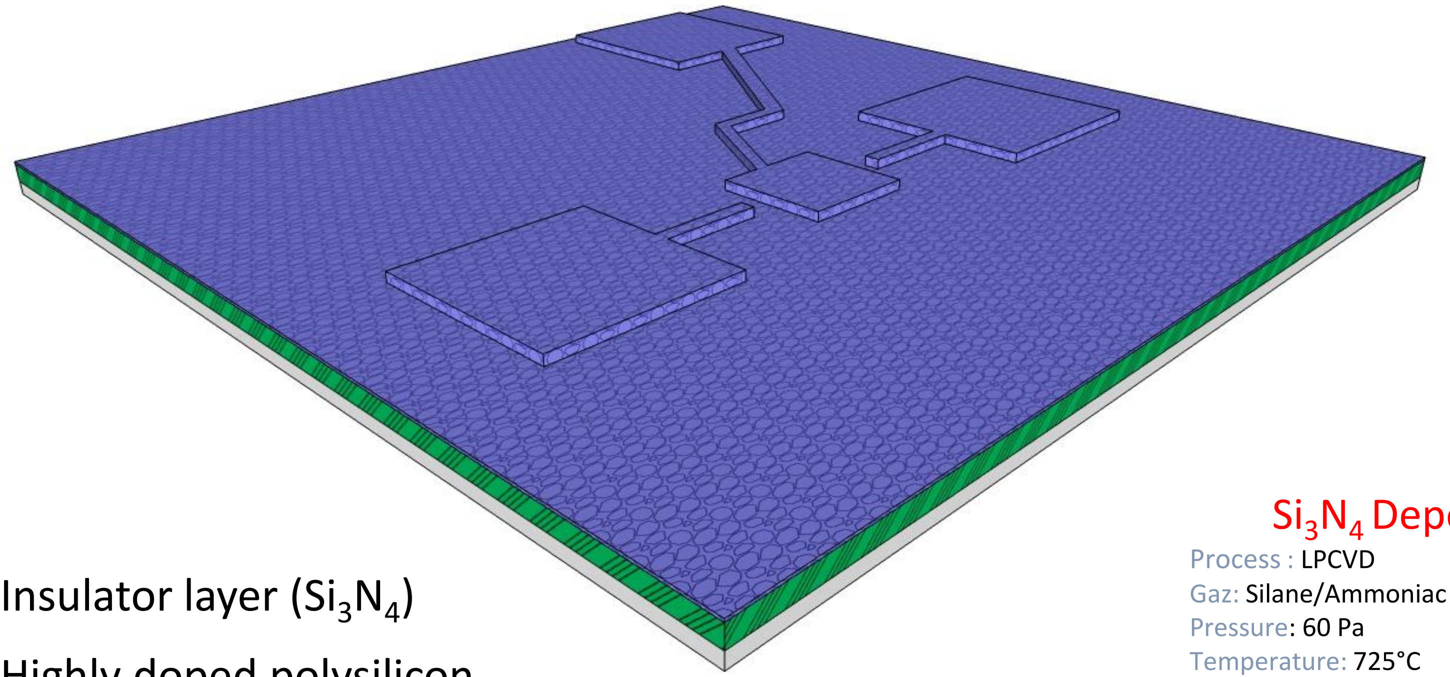
Etching rate: environ 150nm/min

Dual Gate TFT with polysilicon

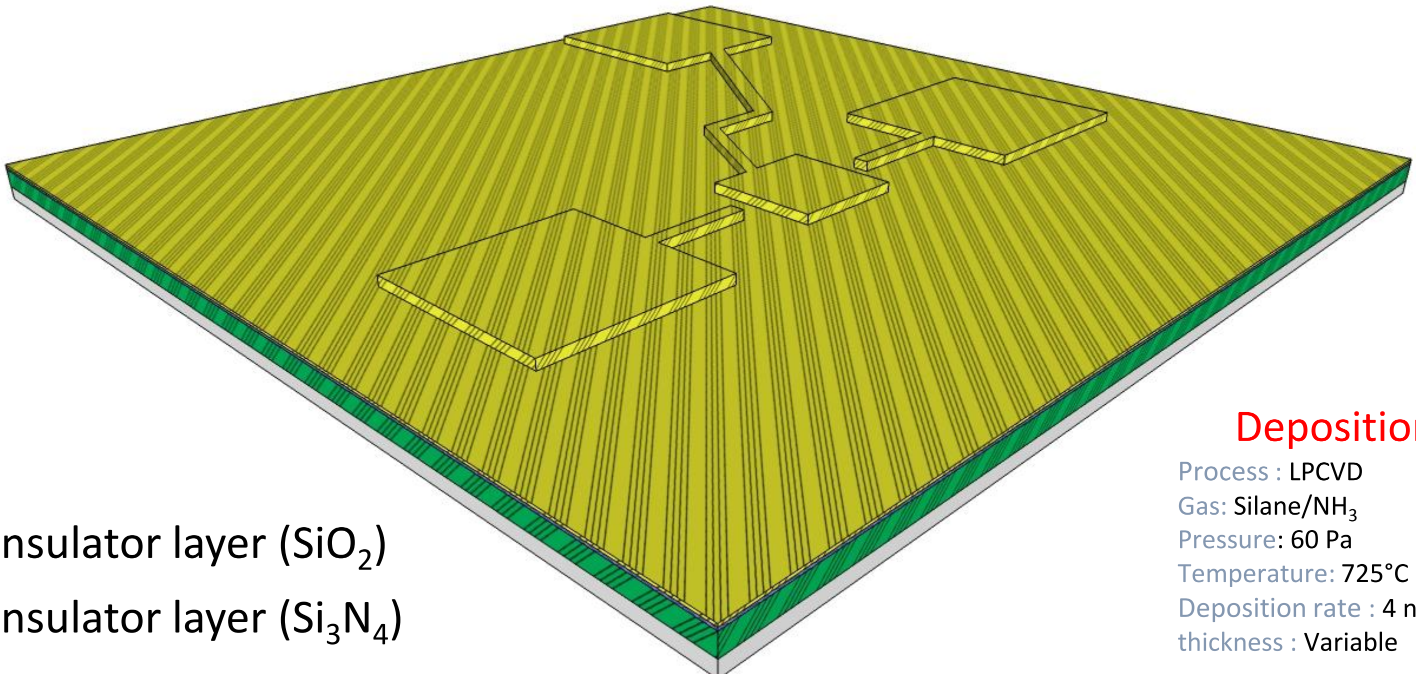


- Insulator layer (Si_3N_4)
- Highly doped polysilicon
- Wafer insulation (silicon oxide)
- Silicon Wafer

Si_3N_4 Deposition

Process : LPCVD
Gaz: Silane/Ammoniac
Pressure: 60 Pa
Temperature: 725°C
Deposition rate : 4 nm/min
thickness : Variable

Dual Gate TFT with polysilicon



- Insulator layer (SiO_2)
- Insulator layer (Si_3N_4)
- Highly doped polysilicon
- Wafer insulation (silicon oxide)
- Silicon Wafer

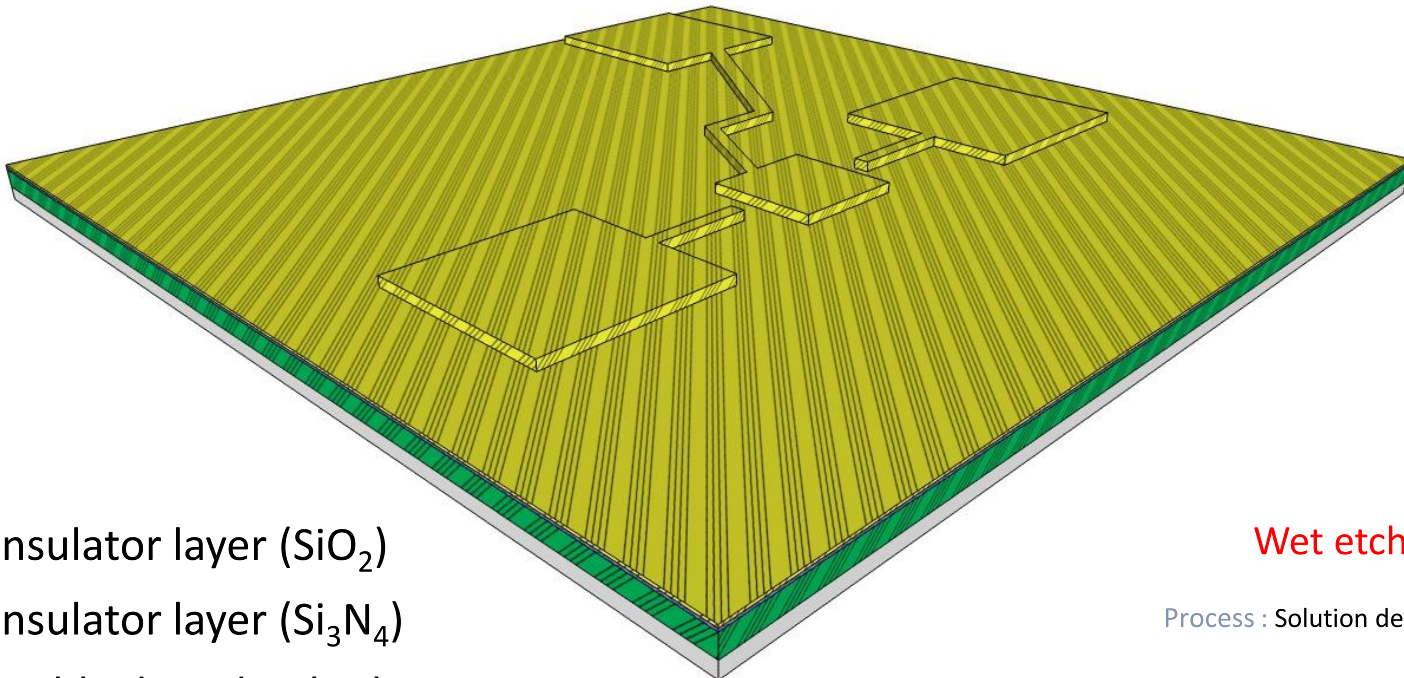
Deposition of Si_3N_4

Process : LPCVD
Gas: Silane/NH_3
Pressure: 60 Pa
Temperature: 725°C
Deposition rate : 4 nm/min
thickness : Variable

Deposition of SiO_2

Process : APCVD
Gas: Silane/Oxygène
Temperature: 420°C
Deposition rate : 29 nm/min
thickness : Variable

Dual Gate TFT with polysilicon



Insulator layer (SiO_2)

Insulator layer (Si_3N_4)

Highly doped polysilicon

Wafer insulation (silicon oxide)

Silicon Wafer

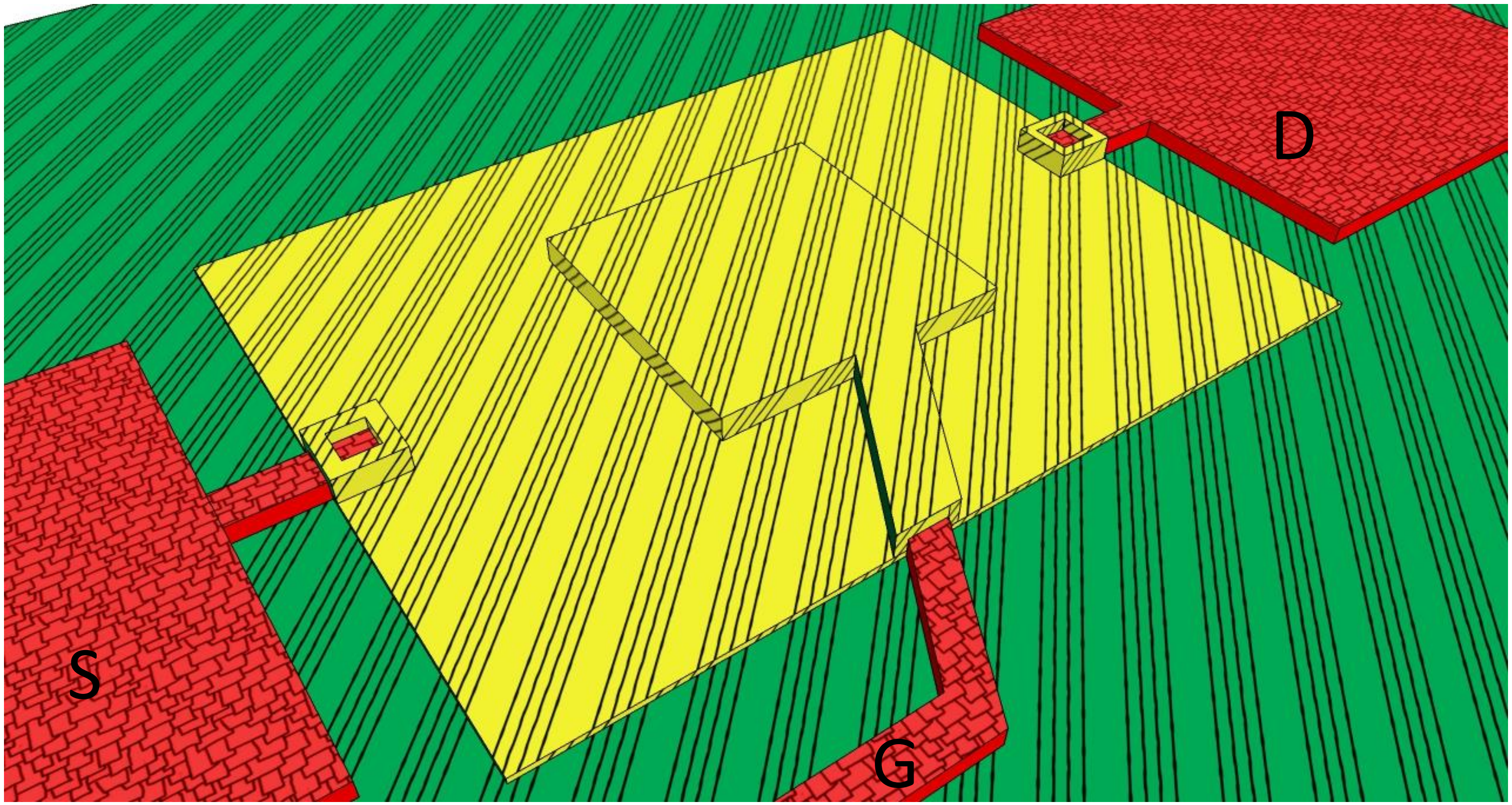
Wet etching of SiO_2

Process : Solution de BHF

Dry etching

Process : Plasma
Power : 30 W
Flow rate: 10 sccm
Pressure: 1 Pa
Etching rate : environ 15nm/min

Dual Gate TFT with polysilicon



- Insulator layer (SiO_2)
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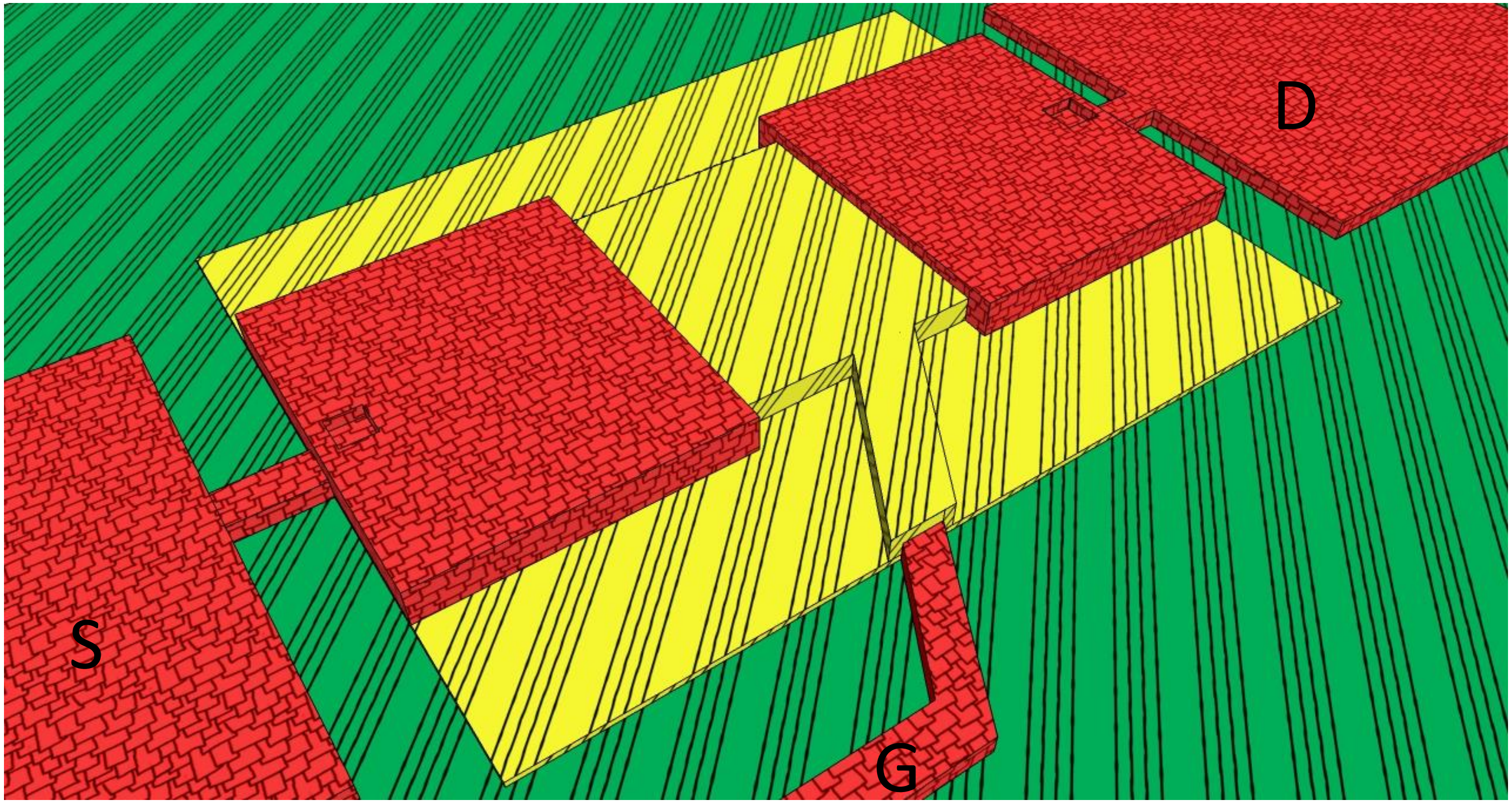
- Wafer insulation (silicon oxide)
- Silicon Wafer

Dual Gate TFT with polysilicon



Insulator layer (SiO_2)

Insulator layer (Si_3N_4)

Highly doped polysilicon

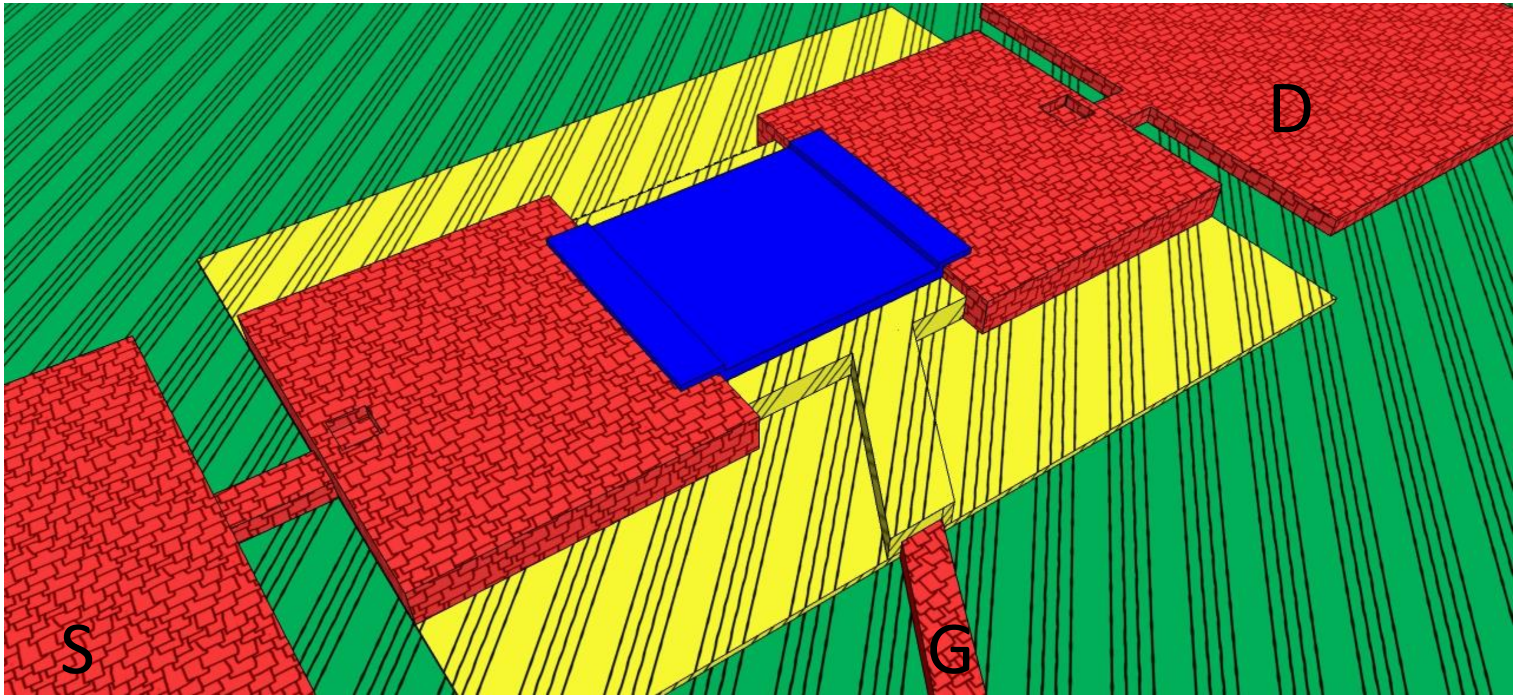
Wafer insulation (silicon oxide)

Silicon Wafer

Doped silicon deposition

Process: LPCVD
Gas: Silane, phosphore
Pressure: 90 Pa
Deposition rate : 5 nm/min
thickness : 300 nm

Dual Gate TFT with polysilicon

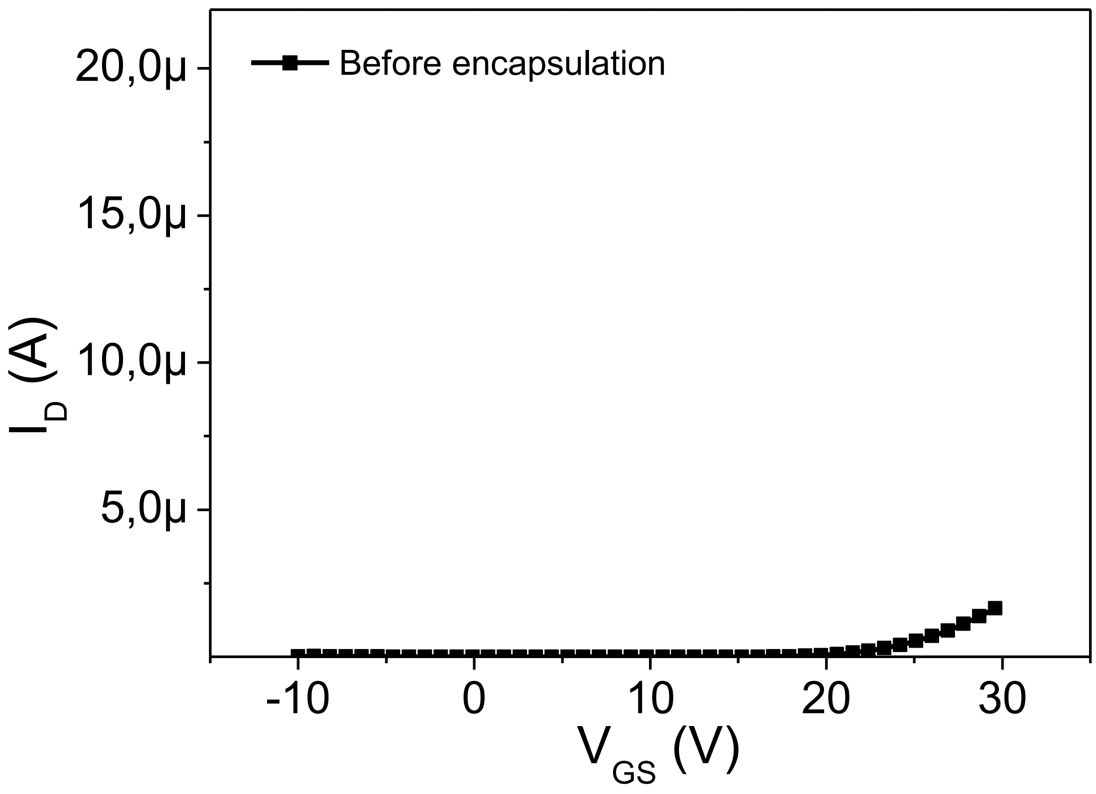


- Poly-silicon
- Insulator layer (SiO_2)
- Insulator layer (Si_3N_4)
- Highly doped polysilicon
- Wafer insulation (silicon oxide)
- Silicon Wafer

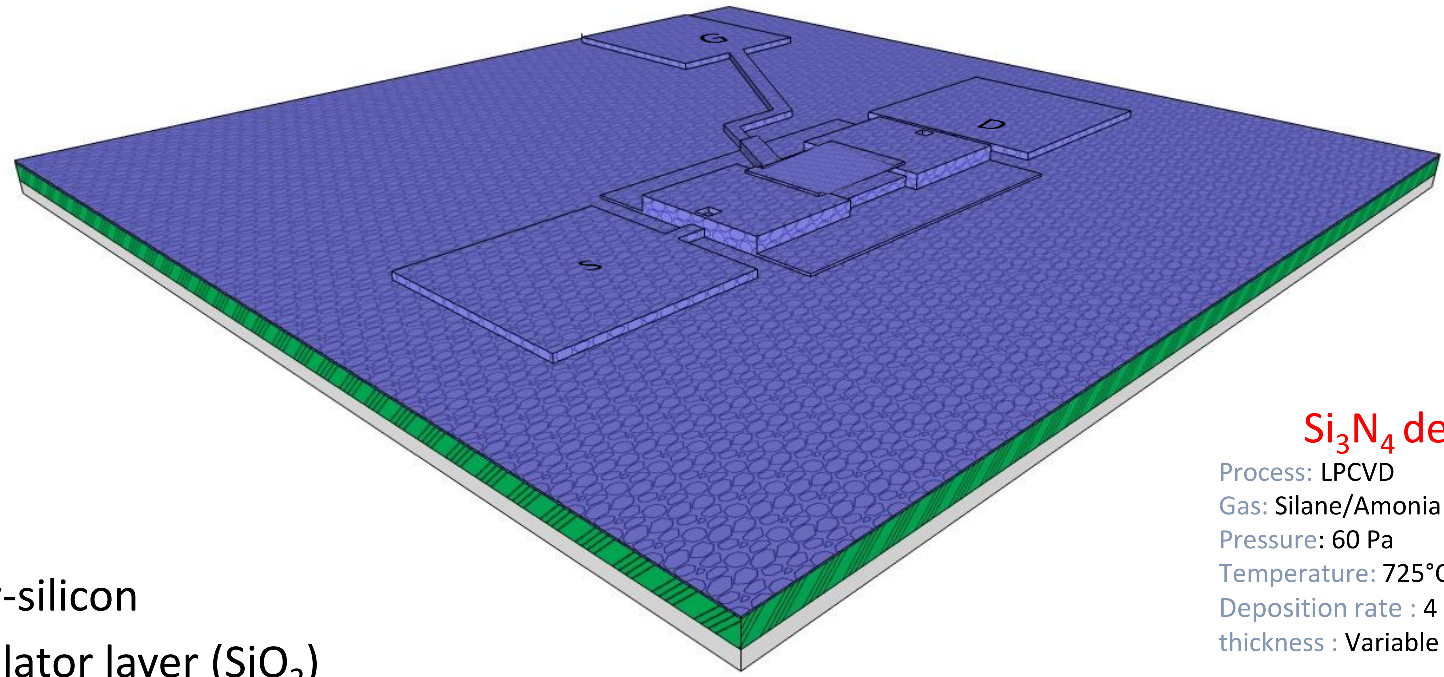
Poly-silicon deposition

Process: LPCVD
Gas: Silane
Pressure: 90 Pa
Deposition rate : 5 nm/min
thickness : 100 nm

First electrical measurement



Dual Gate TFT with polysilicon

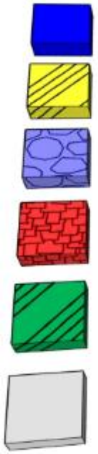


Si_3N_4 deposition

Process: LPCVD
Gas: Silane/Amonia
Pressure: 60 Pa
Temperature: 725°C
Deposition rate : 4 nm/min
thickness : Variable

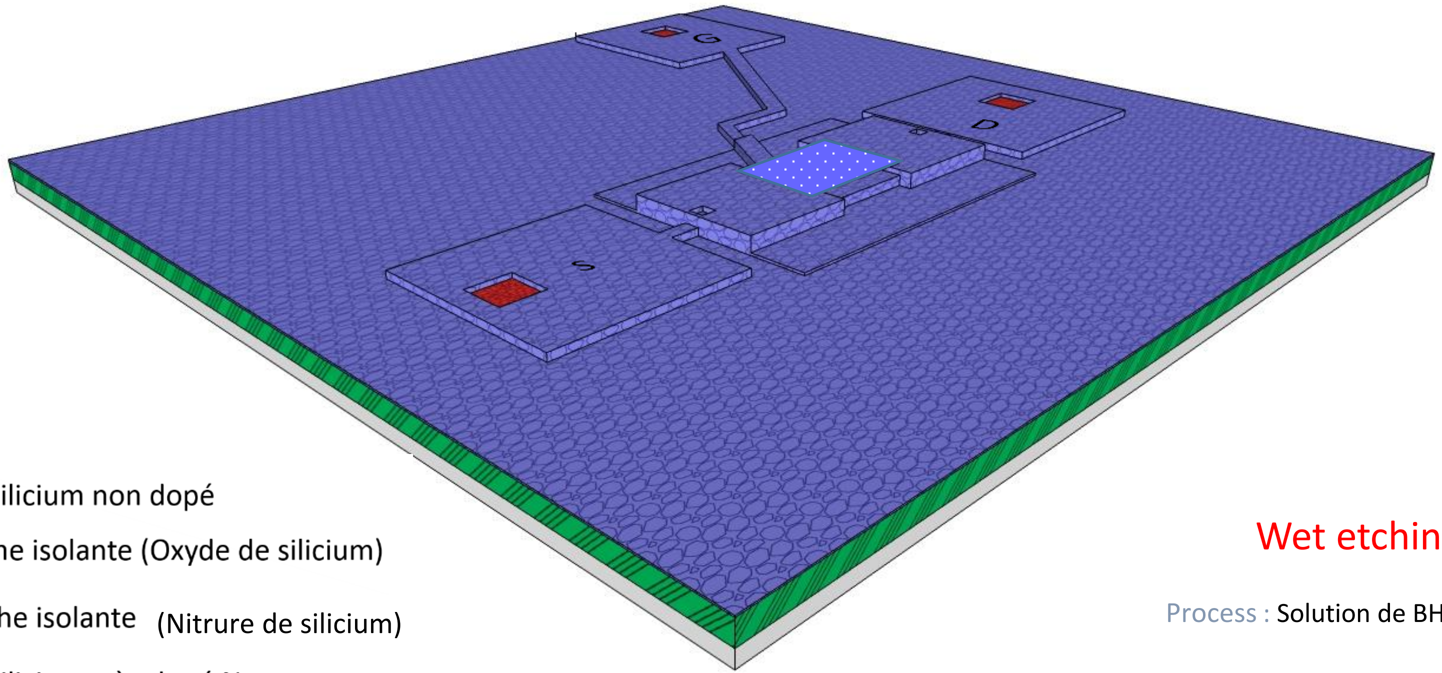
SiO_2 deposition

Process: APCVD
Gas: Silane/Oxygène
Temperature: 420°C
Deposition rate : 29 nm/min
thickness : Variable



- Poly-silicon
- Insulator layer (SiO_2)
- Insulator layer (Si_3N_4)
- Highly doped polysilicon
- Wafer insulation (silicon oxide)
- Silicon Wafer

Dual Gate TFT with polysilicon



- Polysilicium non dopé
- Couche isolante (Oxyde de silicium)
- Couche isolante (Nitrure de silicium)
- Polysilicium très dopé N
- Isolation du wafer (Oxyde de silicium)
- Wafer de silicium

Wet etching of SiO_2

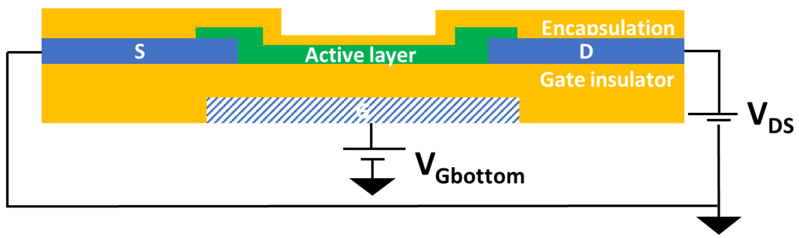
Process : Solution de BHF

Dry etching

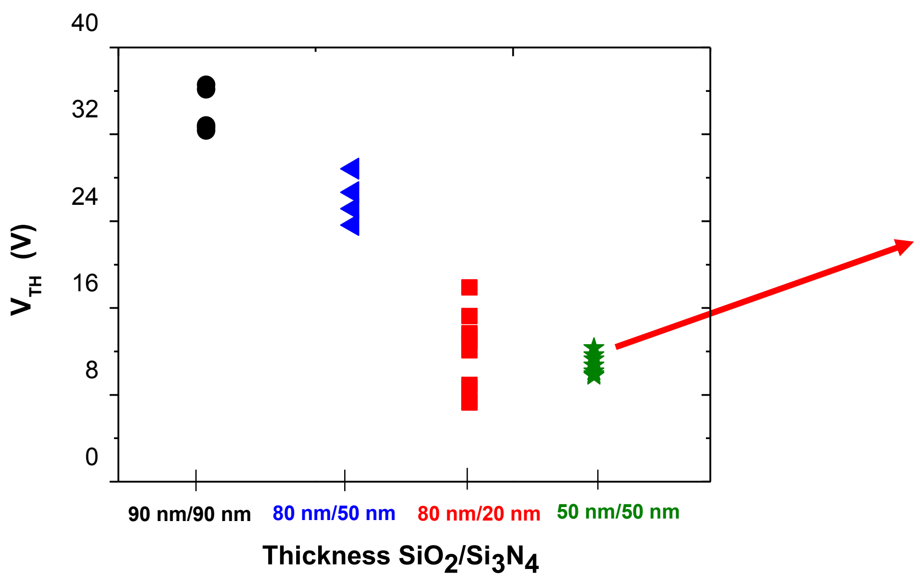
Process : Plasma
Power : 30 W
Flow rate: 10 sccm
Pressure: 1 Pa
Etching rate : environ 15nm/min

Optimization of the bottom dielectric

1rst Goal : decrease of the threshold voltage for bottom gate structure



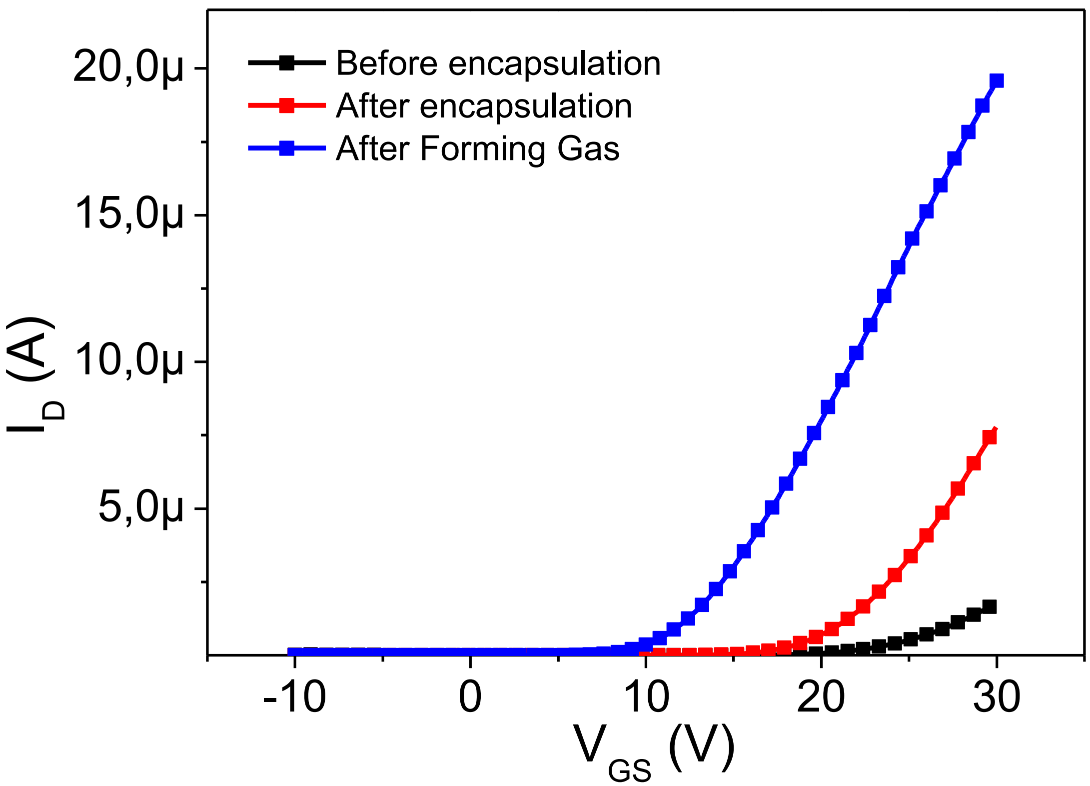
Test with several bottom gate insulators
→ Thicknesses



Best result

- Low threshold voltage
- Low dispersion in data point

Final transfer characteristic



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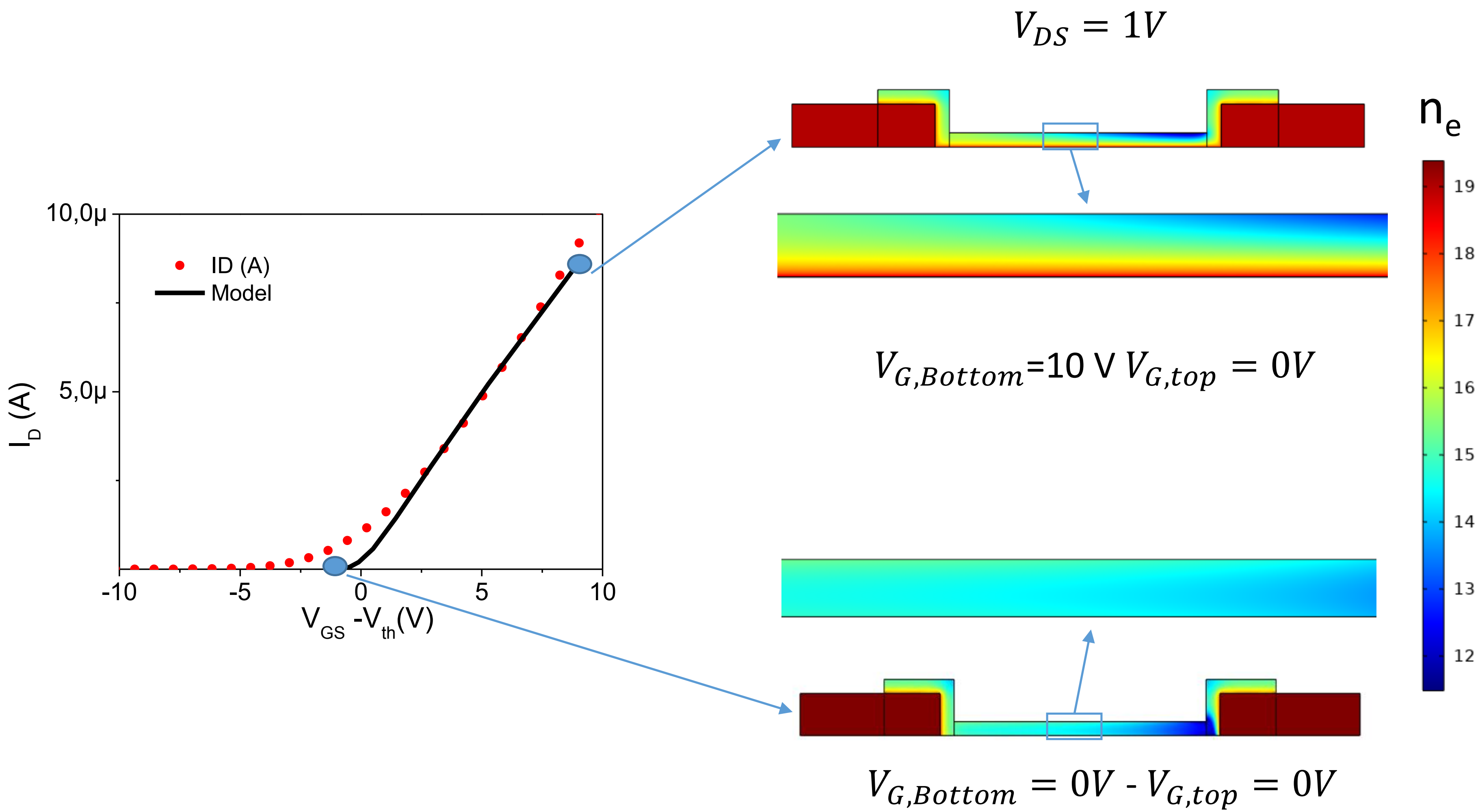
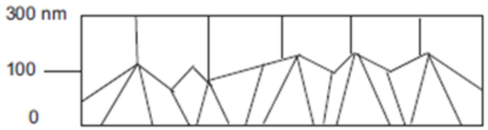
Modeling


$V_{DS} = 1V$
n_e
19
18
17
16
15
14
13
12
10,0µ
5,0µ
ID (A)
Model
I_D (A)
-10
-5
0
5
10
V_{GS} -V_{th}(V)
$V_{G,Bottom}$=10 V $V_{G,top} = 0V$
$V_{G,Bottom} = 0V$ - $V_{G,top} = 0V$

Amplification values

Theoretical amplification calculated from capacitance amplification : $\frac{C_{Top}}{C_{Bottom}}$

Real amplification (for TFT):



Larger grains

Smaller grains

$\mu_{Bottom} \neq \mu_{Top}$

$$I_D = \frac{W}{L} V_{DS}\left[\mu_{Bottom} * C_{Bottom} \left(V_{G,Bottom} - V_{th,Bottom}\right) + \mu_{Top} * C_{Top} \left(V_{G,Top} - V_{th,Top}\right)\right]$$

$$I_D = \frac{W}{L} V_{DS}\left[\mu_{Bottom} * C_{Bottom} \left(V_{G,Bottom} - V_{th,Total}\right)\right]$$

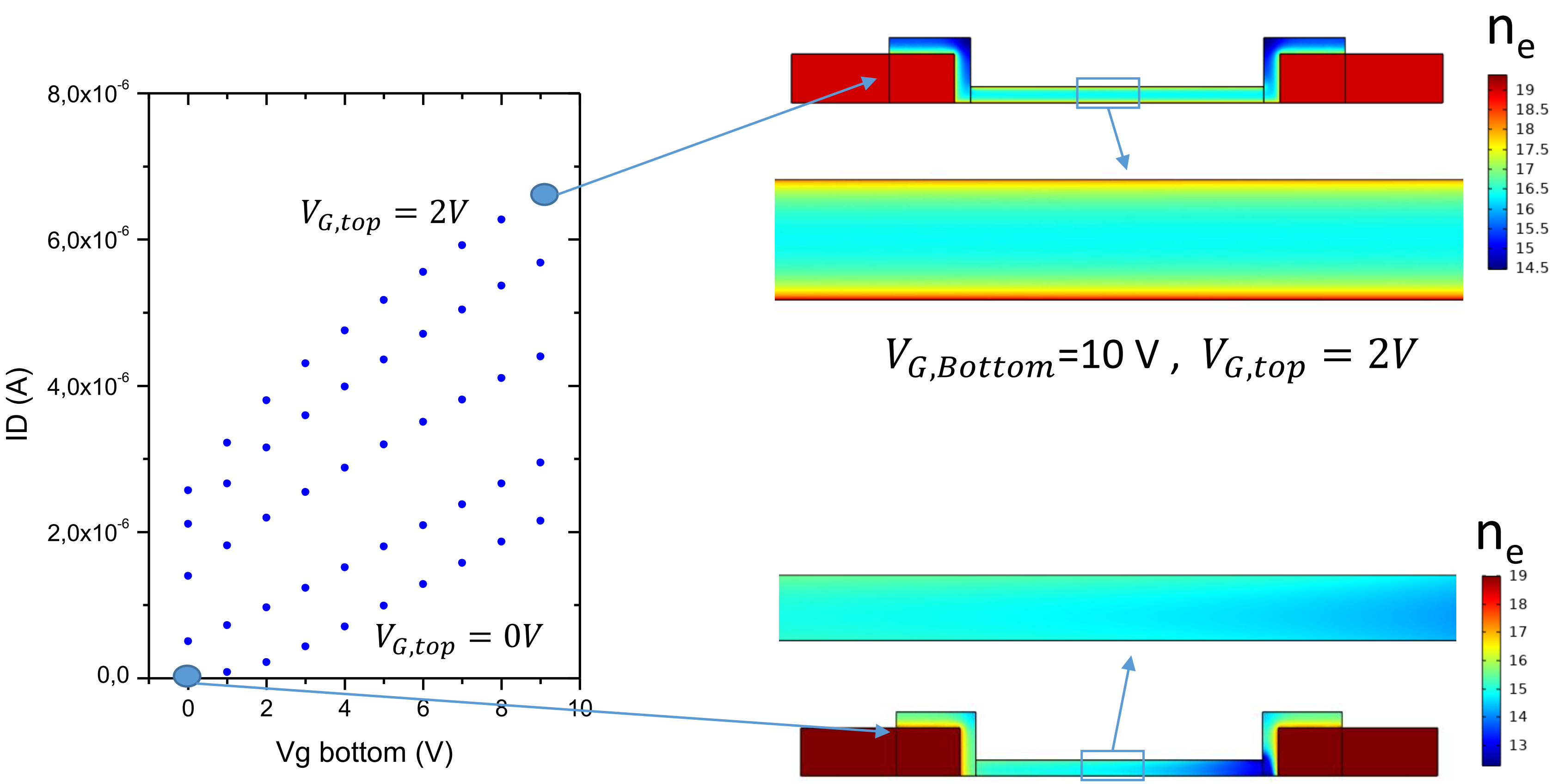
$$V_{th,Total} = V_{th,Bottom} - \frac{\mu_{Top} * C_{Top}}{\mu_{Bottom} * C_{Bottom}} \left(V_{G,Top} - V_{th,Top}\right)$$

$$\Delta V_{th,Total} = \frac{\mu_{Top} * C_{Top}}{\mu_{Bottom} * C_{Bottom}} \left(\Delta V_{th,Top}\right)$$

Sensitivity

Modeling

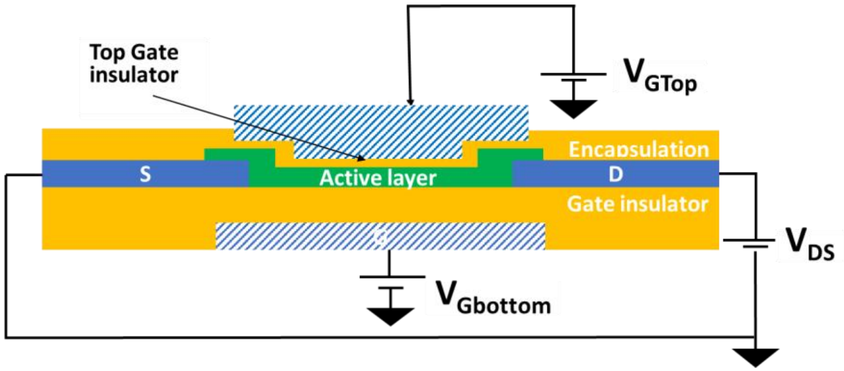
$V_{DS} = 1V$



$V_{G,Bottom}$=10 V , $V_{G,top} = 2V$

$V_{G,Bottom} = 0V$, $V_{G,top} = 0V$

Dual gate operation



Material	ε_r	Thickness (nm)
SiO_2	3.90	50
Si_3N_4	6.90	50
SiO_2	3.90	5,5

$$\epsilon_{eq} = \frac{d_1 + d_2}{\frac{d_1}{\epsilon_1} + \frac{d_2}{\epsilon_2}}$$

$C_{Bottom} = 4{,}4 \times 10^{-8}$ F/cm^2

Active layer : undoped polysilicon 100 nm

Gate layers : highly doped polysilicon

Top gate insulator

- Si_3N_4, 25 nm → $C_{Top} = 8{,}8 \times 10^{-8}$ F/cm^2
- SiO_2, 25 nm

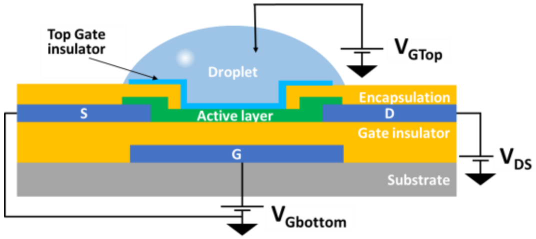
- SiO_2, 5,5 nm (native oxide) $C_{Top} = 6{,}2 \times 10^{-7}$ F/cm^2

Theoretical amplification:

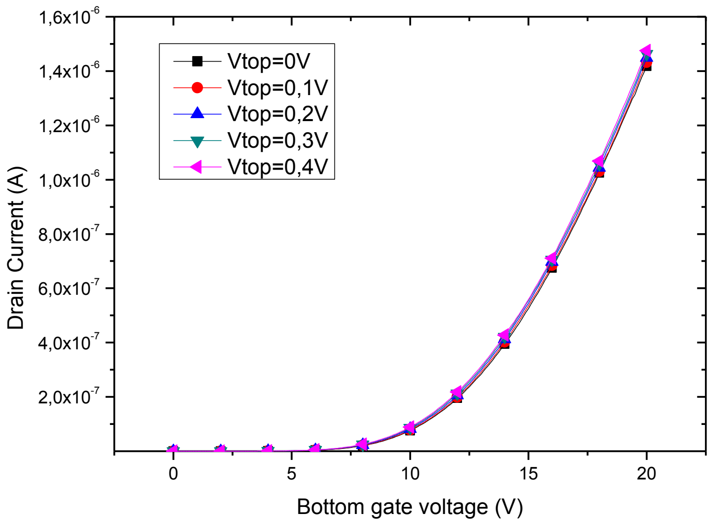
$$\frac{C_{Top}}{C_{Bottom}} = 2$$

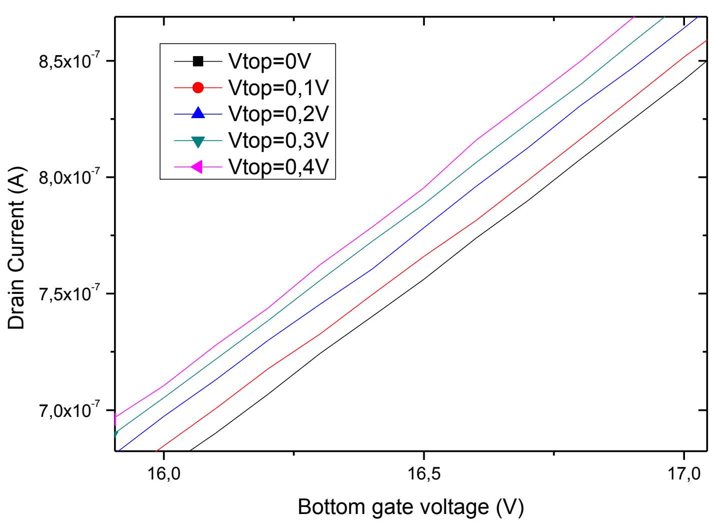
$$\frac{C_{Top}}{C_{Bottom}} = 14$$

Water measurement

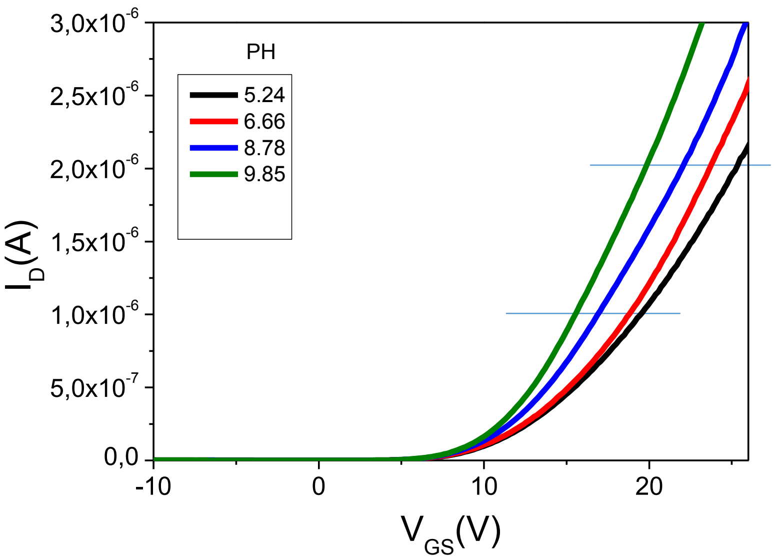


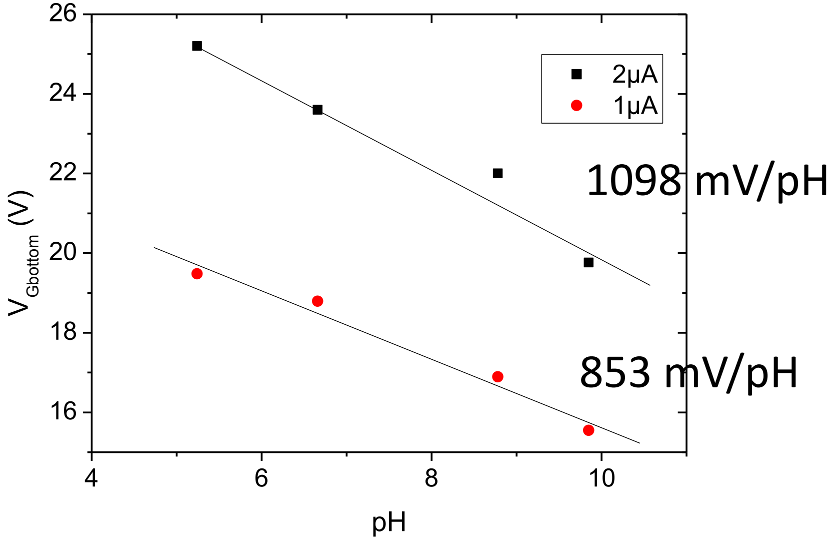
Droplet Polarization





PH measurement (C_{top}->5,5nm)





Amplification factor > 14

Top gate threshold voltage

Possibilities to decrease the top gate threshold voltage

Decrease the top insulator thickness
→ Limitations due to electrical insulation

Increase of the quality of the interface between silicon dioxide and polysilicon
→ Optimization already done

Increase of the quality of polysilicon layer
→ Optimization already done (low temperature process)
→ Many traps at grain boundaries and between interfaces
→ High threshold voltage

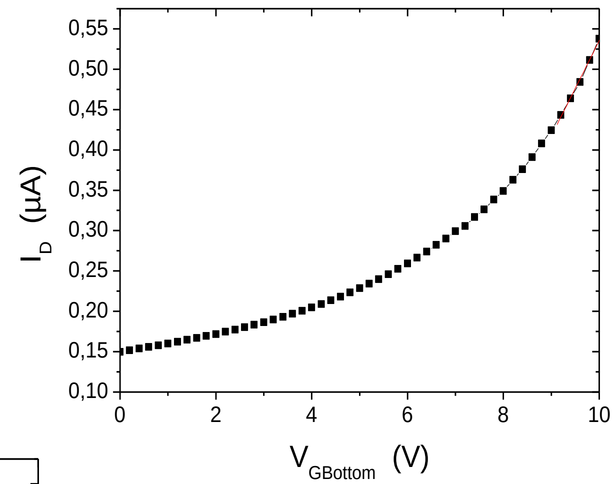
Increase the doping level of polysilicon
→ Modification of the transfer characteristic
→ Increase the conductance

TFT with low doped polysilicon

Active layer :

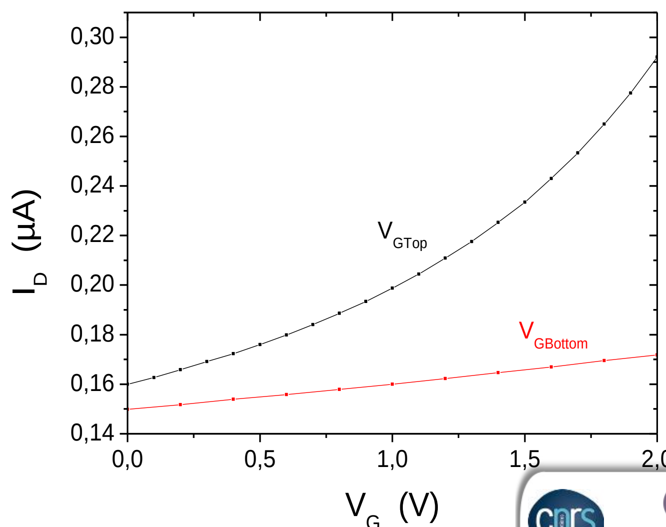
- Polysilicon deposited from silane by LPCVD
- In-situ doping with phosphine (control of the ratio of gases)

➡ Characterization versus Bottom gate



Field effet → Channel conductance
Low On/off ratio → Not important for sensing

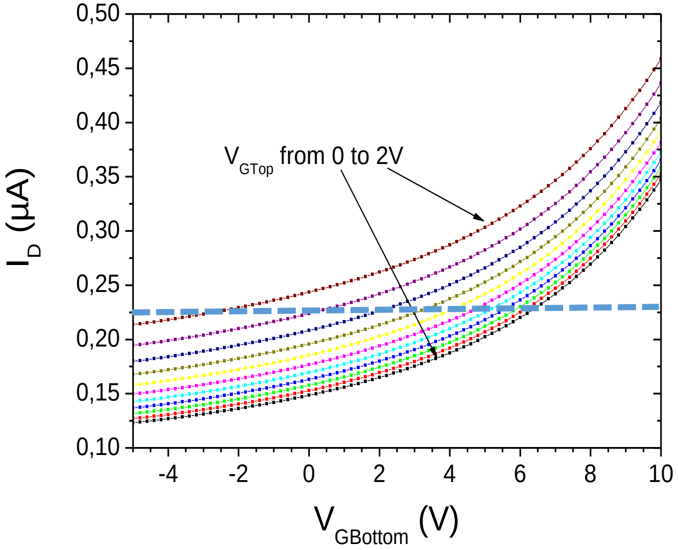
Comparison Top gate versus Bottom gate transfer characteristics

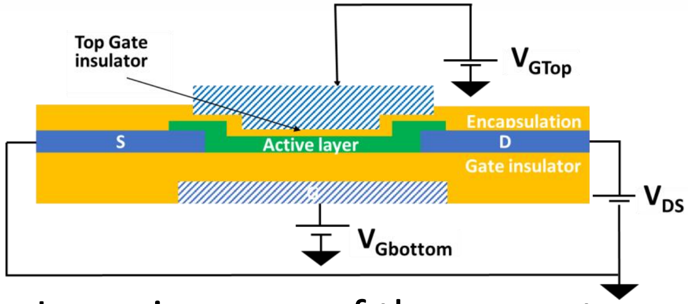


➡ V_{GTop} compatible with tests in liquid

Dual Gate TFT with low doped polysilicon

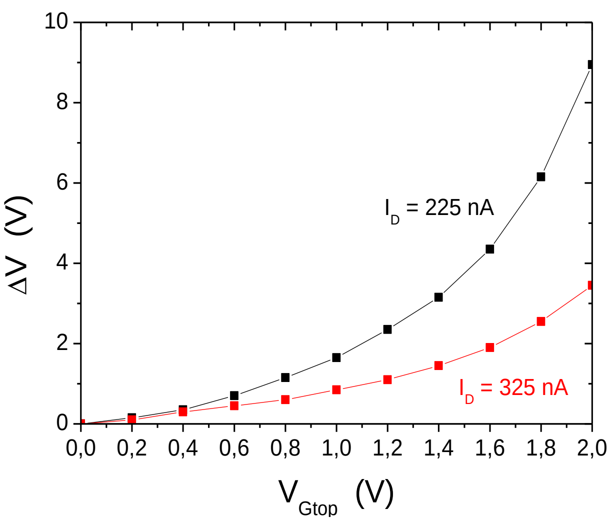
Transfer characteristics versus $V_{GBottom}$
With different values of V_{GTop}





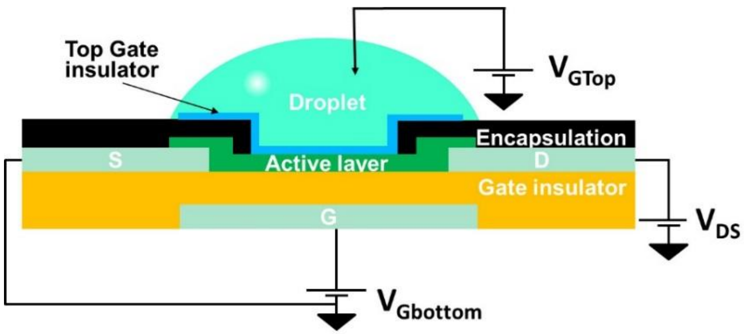
Large increase of the current due to the top channel

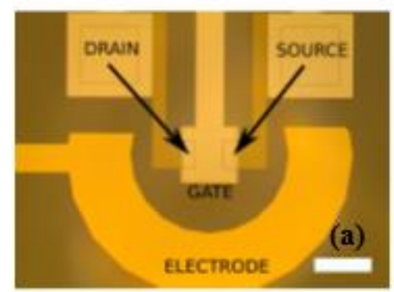
Voltage shift with fixed I_{DS}



The slope gives
the amplification ratio

Measurements in liquids



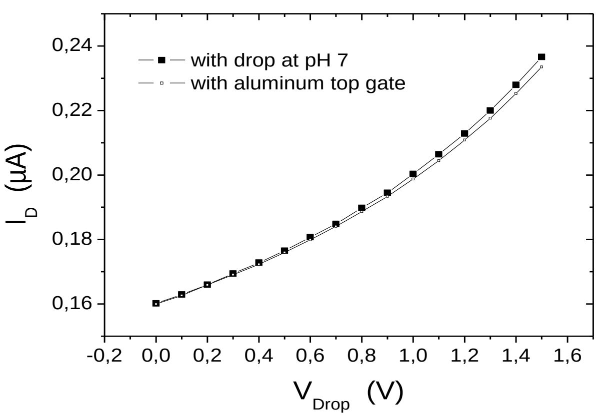


Top Gate with polarized droplet → Metallic electrode (Ti/Au) for Top gate

Comparison of transfer characteristics

- With metallic Gate (Al)
- With liquid Gate

⇒ Good correlation showing the good functioning in liquid media



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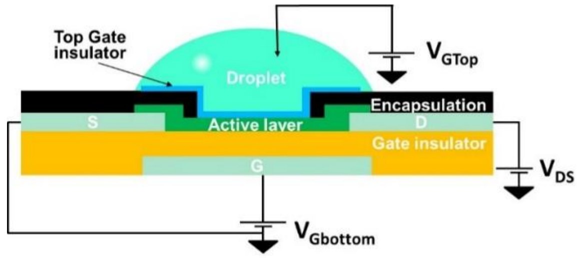
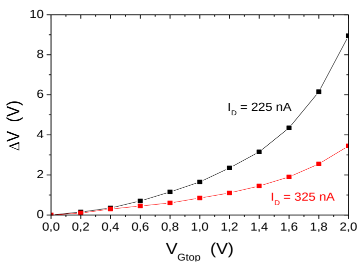
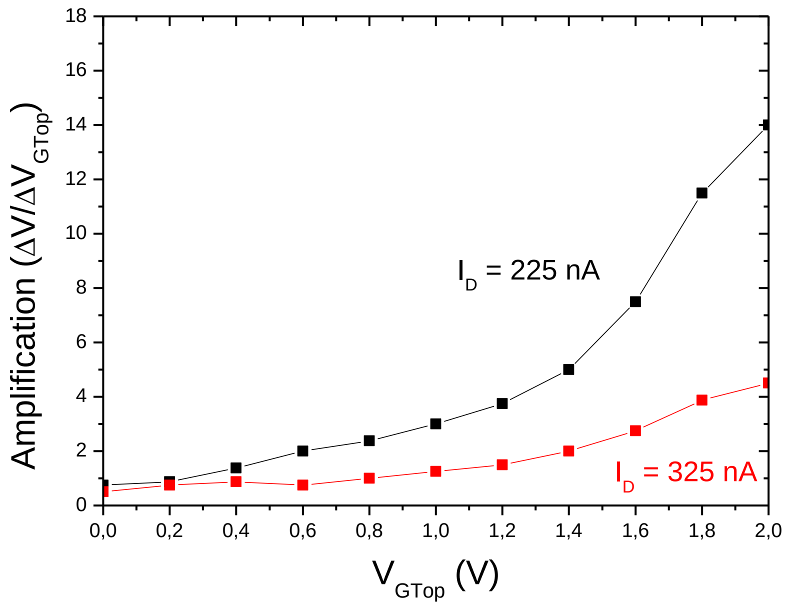
Amplification versus polarization







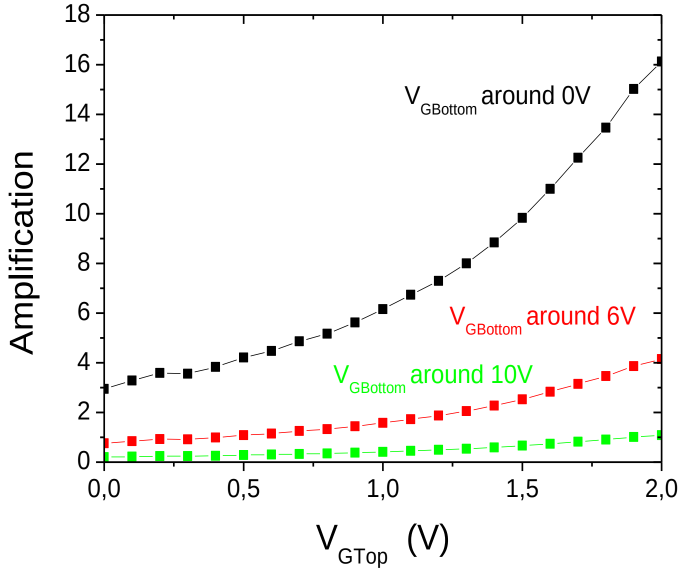
The amplification value increases with V_{GTop} → Top channel formation

The amplification value is higher at low $V_{GBottom}$ → Top channel more influent than Bottom channel

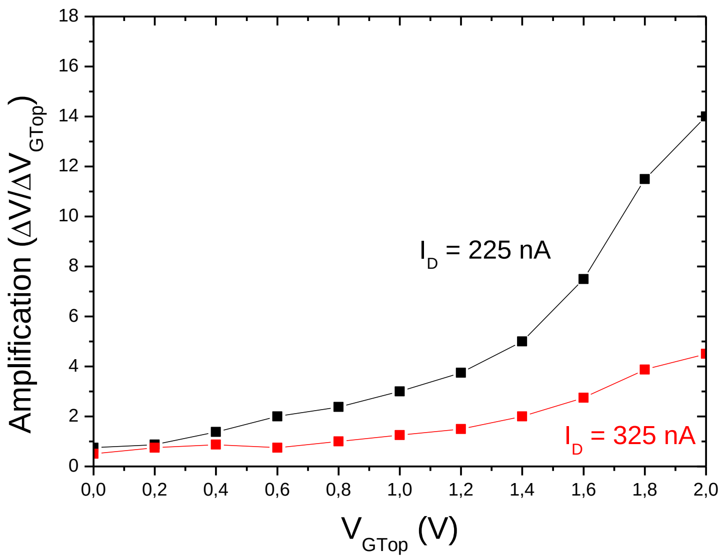
Measured amplification >> Calculated amplification (C_{Top}/C_{Bottom})

Comparison of Amplification values

Theoretical values



Measured values



Amplification range consistent with theory

Increase of the amplification with polysilicon layers

Conclusion : Measurements in liquids

Several tests with solutions with various pH values

→ Sensitivity above the Nernst value > 59 mV/pH

→ Highly dependent on polarization

→ The sensitivity is higher for low bottom gate voltage (under 4V) and increases with the top gate voltage.

→ consistent with previous calculated and measured amplification values in dual gate configuration

Examples :

Amplification factor with :

- $V_{GBottom}$ around 3
- V_{GTop} = 0.75V

→ 3.5

→ pH sensitivity around 200 mV/pH

Amplification with :

- $V_{GBottom}$ around 3
- V_{GTop} = 0.5 V

→ 2.6

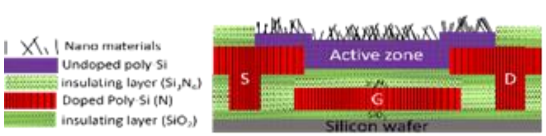
→ around 150 mV/pH

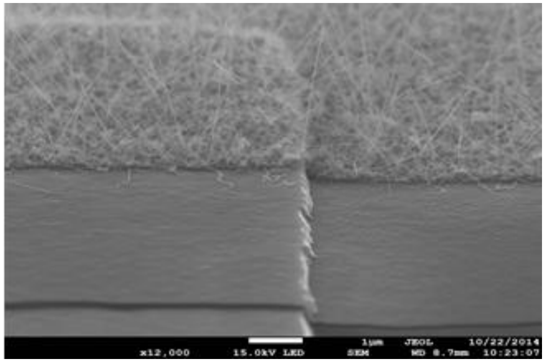
Prospects :Applications to biodetection

- Very promising results with pH
    - Application to bio elements

- Integration of nanomaterials on the top surface
    - Nanowires, nanotubes, nanocarbons (porous)

- Create a structure based on Extended gate TFT





Increase the surface
And interactions
with biomolecules

Acknowledgment : ANR PlasBioSens

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Sensor for biodetection

- Easy measurement
- Integrated

Electronic detection

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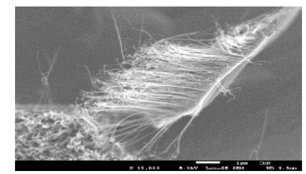
- Highly sensitive → Sensor sensitivity
  - → Surface
  - → Nanomaterials



- High selectivity

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Functionalization:
- Chemical
- Biological

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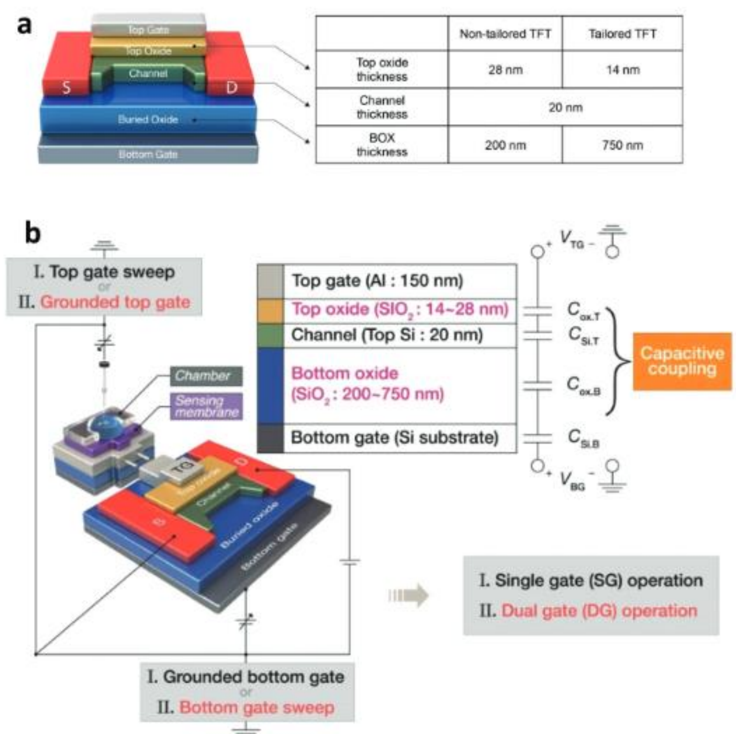
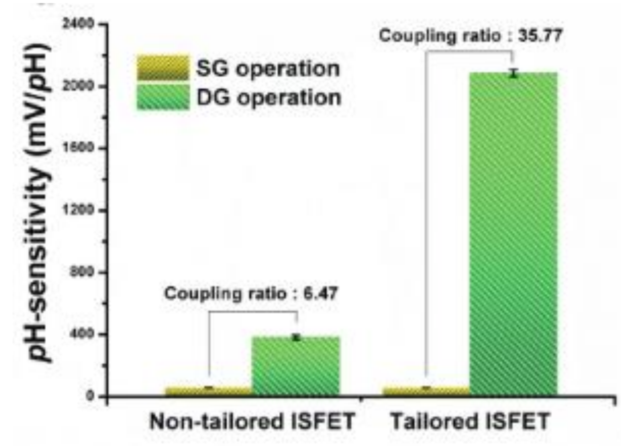
Thank you for your attention

DGFET : Example 1

A self-amplified transistor immunosensor under dual gate operation: highly sensitive detection of hepatitis B surface antigen
Lee *et al*, Nanoscale 7(40):16789, 2015

- SOI (Silicon on Insulator) for the active layer
- Silicon dioxide a s insulator
- Extended gate





Application to biosensing
Antigen / Antibody links

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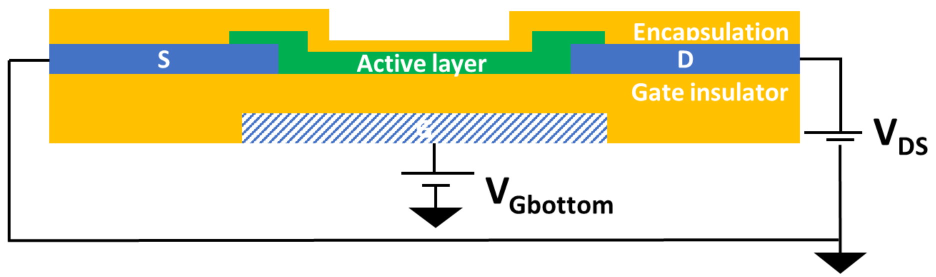
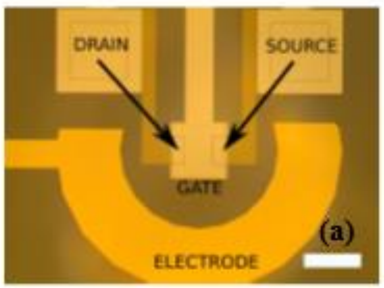
Dual Gate TFT with polysilicon

Final structure



External top gate contact



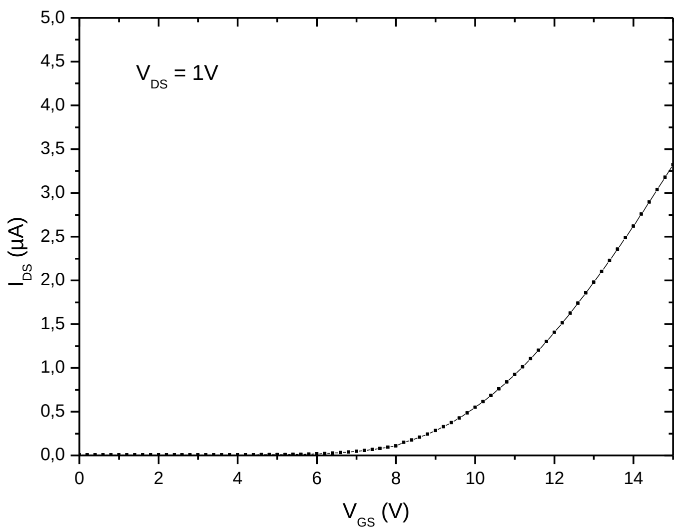
Deposition of a top gate contact (aluminum) ➡ Top gate / Bottom gate / Dual gate — Characterization

➡ Capacitive amplification

Characterization with liquid (pH sensor) : with deported electrode (Au/Ti)

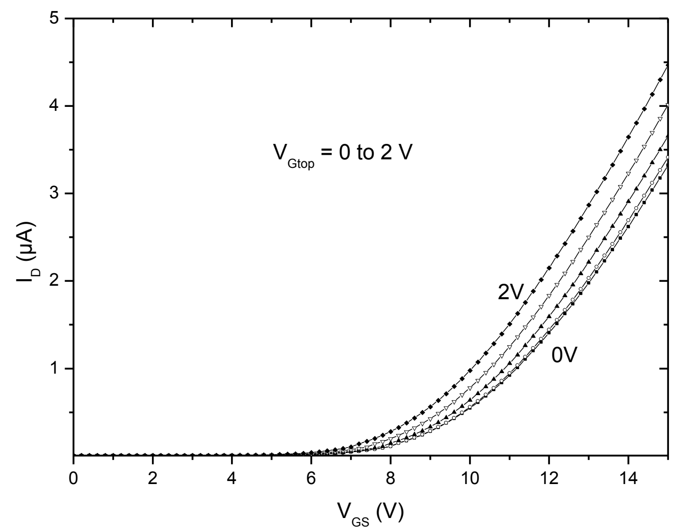
Characterization : Bottom gate

Transfer characteristic



Mobility μ_{FE} (cm2/V.s)	Threshold voltage V_{th} (V)
12,5	10

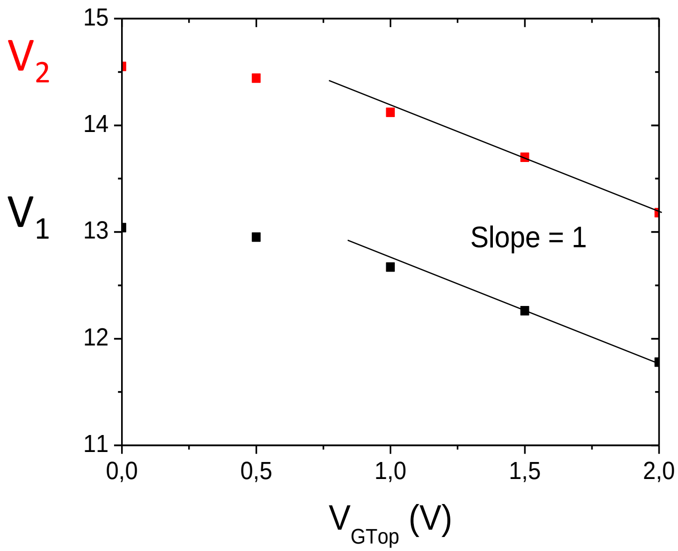
Dual Gate Characteristics



I_{DS} ↗ with V_{GTop}

Dual Gate Characterization

I_{DS} fixed to 2 µA or 3 µA



For each V_{GTop}:

$V_1 = V_{GBottom}(I_{DS}=2\ \mu A)$

$V_2 = V_{GBottom}(I_{DS}=3\ \mu A)$

→ Effect for V_{GTop} > 1V

Slope = 1 → $\Delta V = \Delta V_{GTop}$

No capacitance amplification → Potential shift

→ Top Gate threshold voltage to high